

NRA-99-05-OSS-0078

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**NRA 99-OSS-05 - Advanced Cross Enterprise Technology Development for NASA Missions**

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**Proposed Principal Investigator:**

Dr. Dariush Divsalar  
JPL  
238-420  
4800 Oak Grove Dr.  
Pasadena, CA 91109-  
818-393-5138(phone)  
818-354-6825(fax)  
dariush@shannon.jpl.nasa.gov

PI Signature and Date:

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**Institution Authorization**

Name of Authorizing Official:

Title:

Institution:

Signature and Date:

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**Full Title**

Power and Bandwidth Efficient Coded Modulation for Very High Data Rates

**Short Title:** Power and Bandwidth Efficient Coded Modulation

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**Requested Funding & Duration**

Year One: \$ 414,000  
Year Two: \$ 352,000  
Year Three: \$ 329,000

Total: \$ 1,095,000

Duration: 3 years

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**Co-Investigators/Collaborators**

Dr. Fabrizio Pollara  
-- Jet Propulsion Laboratory  
-- Co-Investigator  
-- Email: fabrizio@shannon.jpl.nasa.gov

Dr. Kenneth Andrews  
-- Jet Propulsion Laboratory  
-- Co-Investigator

-- Email: andrews@shannon.jpl.nasa.gov

Dr. Samuel Dolinar

-- JPL

-- Co-Investigator

-- Email: sam@shannon.jpl.nasa.gov

Dr. C. Wayne Walker

-- TRW Electronics and Technology Division

-- Co-Investigator

-- Email: Wayne.Walker@trw.com

Prof. Robert McEliece

-- California Institute of Technology

-- Co-Investigator

-- Email: rjm@systems.caltech.edu

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**NASA Grant or Contract Number of any current NASA award that the PI holds that is a logical predecessor of the newly proposed work**

**Type of Proposing Institution:** NASA Center

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**Enterprise(s)**

**Enterprise 1:** ESE

**Enterprise 2:** SSE

**Enterprise 3:** HEDS

**Enterprise 4:**

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**Thrust Area:** High Rate Data Delivery

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**Education Component Included?** Yes

**Requested Education Funding:**

Year One: \$ 7,500

Year Two: \$ 7,500

Year Three: \$ 7,500

**Total Education Funding:** \$ 22,500

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**Proposal Summary (Abstract)**

In many space environments, power and bandwidth are precious resources, and high data rate communication requires powerful bandwidth-efficient coded modulation methods. The objective of this proposed work is to combine recently developed turbo coding concepts with high-level, bandwidth-efficient modulation techniques to create high data rate coded modulation systems that will enhance the data throughput in any cross-enterprise mission subject to power and bandwidth limitations.

Recently developed turbo codes now represent the state of the art in error correcting codes, yet the primary application of these codes up to now has been Binary Phase Shift Keying (BPSK). Superior modulation schemes for bandwidth efficiency include Trellis Coded Modulation (TCM) and Continuous Phase Modulation (CPM). We propose to combine turbo coding concepts with TCM, and to explore a new concept of turbo coded CPM, for applications requiring high spectral efficiency and constant envelope

modulation. Turbo-TCM (TTCM) started at JPL in 1995-96. There is now extensive external literature, but no implementations. Current results do not point to a clearly winning method, especially when the tradeoff includes complexity and decoding speed, besides power and bandwidth efficiency. Turbo-coded CPM is a novel concept.

As extensions of the original turbo coding concepts developed in 1993, JPL pioneered the development of lower complexity "turbo-like" codes for BPSK. We now have a unique opportunity to extend these low-complexity turbo-like codes to higher level modulations for bandwidth efficiency. We are also proposing a new parallel architecture TTCM concept that can be used with high-level modulation schemes such as MPSK and MQAM. The parallel architecture will allow the use of simple binary decoders capable of very high speed operation.

We will also develop decoder architectures for these codes. Present decoders exist only for BPSK modulation at moderate speeds (<1 Mbps). There is an opportunity to take advantage of the newly developed low-complexity turbo-like code structures, and of parallel decoding architectures, to design advanced decoders suitable for very high data rates.

The work falls into three areas of investigation: Turbo Trellis Coded Modulation (TTCM) development, turbo coded CPM research, and very high-speed digital demodulator and decoder design.

1. TTCM is expected to combine the excellent coding gains from turbo codes with the bandwidth efficiency of traditional TCM. Investigations will rely on the use of linear bandwidth efficient modulations (e.g. pulse-shaping and higher order modulations, such as 8PSK, 16QAM, and 32QAM). The new parallel architecture concept will be applied for highest performance and decoding speed. Decoder complexities will be evaluated through comparison with decoders for convolutional codes.

2. Turbo coded CPM represents a completely new concept in combining modulation and serially concatenated codes. One of the codes will be represented by the memory in the CPM waveform. This technique is similarly applicable to filtered signals that exhibit intersymbol interference.

3. High-speed digital demodulator/decoder design will build upon advances in high speed demodulator technologies.

Modifications to iterative decoding architectures will be examined to increase decoding speed while minimizing impact on performance.

Performance in terms of power and bandwidth efficiency, and of decoding complexity will be demonstrated on a software simulation testbed, which will also enable comparisons among different schemes.

Results will be documented in a comprehensive research report, including quantitative comparisons between the coded modulation methods examined, which will be demonstrated on the software simulation testbed. Publication of several peer-reviewed journal articles is expected in the course of this work. The final output will be a recommendation for selected coded/modulation schemes, with tradeoffs and an implementation plan.

The bandwidth-efficient coded modulation methods proposed here will benefit virtually all terrestrial and Earth-orbiting communication systems (Earth Science Enterprise), where both power and bandwidth are almost always limited. Future Mars missions will also require very high data rates and will have to compete with increasingly stringent spectrum allocations for space exploration (Space Science Enterprise). The proposed coded modulation technology will yield communication system components of smaller size and mass, which will benefit the Human Exploration and Development of Space Enterprise. Our new coded modulations are expected to outperform the best existing TCM approaches, saving at least 2 dB in power requirements or increasing throughput by at least a factor of 1.5 without any increase in bandwidth.

#### Certification of Compliance with Applicable Executive Orders and U.S. Code

By signing and submitting the proposal identified in this Cover Sheet/Proposal Summary, the Authorizing Official of the proposing institution, as identified above (or the individual proposer if there is no proposing institution):

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## Power and Bandwidth Efficient Coded Modulation for Very High Data Rates

(NRA 99-OSS-05 - February 14, 2000)

*D. Divsalar (P.I.), F. Pollara, K. Andrews, S. Dolinar, R. McEliece, C.W. Walker (Co-Is)*

### 1 Summary of Personnel Commitments and Costs

	First Year		Second Year		Third Year	
	WY	Salary \$K	WY	Salary \$K	WY	Salary \$K
D. Divsalar (PI)	0.65	117	0.52	94	0.47	84
F. Pollara (Co-I)	0.18	32	0.17	30	0.14	25
K. Andrews (Co-I)	0.52	93	0.45	81	0.42	76
S. Dolinar (Co-I)	0.45	81	0.30	54	0.26	47
R. McEliece (Co-I)	0.20	36	0.20	36	0.00	0
W. Walker (Co-I, TRW)	0.31	55	0.32	58	0.54	97
<b>Total</b>	<b>2.30</b>	<b>414</b>	<b>1.96</b>	<b>352</b>	<b>1.83</b>	<b>329</b>

**Table 1**

## 2 Technical/Management Section

### 2.1 Summary

An enduring technical challenge for space-based Earth observation systems and for future planetary science missions is the efficient transport of data at high rates from space to terrestrial ground stations. In the design of these systems, a careful balance is required to operate within pre-determined constraints on bandwidth and power. *This proposal addresses the need for power and bandwidth efficient coding and modulation schemes for transfer of data through high-speed wireless data links from satellite to ground. These new methods improve the state-of-the-art by operating close to the ultimate limits of channel capacity, while requiring an implementation complexity that is low enough for very high data rates by using a novel iterative demodulation/decoding scheme.*

We propose to develop new methods for bandwidth efficient coding. These methods will leverage on the recent research done at JPL on parallel and serial concatenated low-memory convolutional codes for binary phase shift keying (BPSK) modulations with iterative decoding (i.e., turbo codes). These codes have shown very large gains at low code rates for deep-space applications.

A natural extension of these techniques would merge either trellis coded modulation (using high order memoryless modulation and pulse shaping for high throughputs), or high level continuous phase modulation (which has memory and is much less susceptible to the impairments of non-linear amplification, e.g., saturated TWTAs or SSPAs) with low-complexity turbo-like codes. This will achieve similar coding gains in concert with bandwidth efficiency for high data rate satellite to ground communications.

Iterative decoding architectures for the above coded modulation schemes will be designed to achieve high decoding speeds ( $> 1$  Gbps) with minimal sacrifices in performance. These new codes are expected to outperform the best current trellis coded modulation approaches by at least 2 dB for large block sizes. Lower transmitter power implies lower mass and lower launch cost, or higher data rate, or less stringent requirements on the ground stations (A 1 dB improvement in the Deep Space Network ground stations is valued at approximately \$80M).

### 2.2 Objectives and Expected Significance of the Proposed Development

The objective of the research presented in this proposal is the development and analysis of novel modulation, coding and signal processing technologies that will support the deployment of high rate, bandwidth efficient, communications systems operating in a power constrained environment such as satellite to ground communication links. In the following, we outline several research components that will yield a comprehensive understanding of the performance benefits provided by state-of-the-art and novel developments in combined modulation and coding. In addition to the efficiency gains to be obtained in the coding arena, another specific area will focus on high-speed signal processing architectures that address the future implementation of various demodulation/decoding techniques. A system level overview will also address issues related to realistic, linear and non-linear modeling and insure unbiased comparisons between differing solutions to the goal of efficient high data rate communications.

The significance of the proposed new technology for the Space Science and Earth Science Enterprises will be a major improvement in high data rate delivery, in terms of system throughput and/or of reduced requirements on the transmitter power, thus enabling more efficient spacecraft designs. Specifically, the required transmitter power will be reduced by at least 2 dB with respect to the current state-of-the-art, and the throughput will be extended beyond the current capability of 2 bits per transmitted symbol to cope with future spectrum allocation restrictions.

The “Human Exploration Development of Space” Enterprise will also benefit due to its need of enabling higher data throughput, and lower mass /size components.

### 2.3 Technical Approach and Methodology

In order to design a communication system with high throughput, in terms of bits per signaling interval, it is necessary to resort to high order modulations. However, when the additional constraint requiring constant envelope signal sets is in effect, the choice of possible modulations becomes very limited (8 PSK being usually the practical limit).

This study, in addition to developing new coded modulation systems, will consistently address the crucial tradeoffs between restricting the design to constant envelope modulations or allowing higher order non-constant envelope modulations (e.g., 16QAM and higher), accounting, in this case, for the necessary back-off of the power amplifier (to minimize distortion and spectral regrowth).

This study will also address important issues for achieving higher spectral efficiency, involving tradeoffs between increasing the modulation order or applying heavier filtering or pulse shaping. Second order effects altering the constant envelope property due to filtering will also be considered.

Continuous phase modulation (CPM), which is part of this proposal, is obtained by filtering affecting only the phase and hence resulting in constant envelope modulation. Thus CPM can operate at the saturation point of the power amplifier for highest efficiency. To achieve very low side-lobes, specific *spectral coding* techniques (see for example [1]), which create correlation between symbols prior to modulation, will also be considered and compared to CPM<sup>1</sup>.

Finally, another important issue for the design of high data rate systems is the joint use of an efficient parallel architecture for the decoder in conjunction with very low-complexity but high-performance codes, a field where JPL is at the forefront.

### 2.4 Description of Proposed Technology

We address several distinct areas of investigation that will provide NASA's Earth and Space Science Enterprises with advanced power and bandwidth efficient techniques. (1) Turbo Trellis Coded Modulation - Current turbo code research for deep-space communications done at JPL [5] has demonstrated the capability of achieving near-Shannon-limit performance, while simultaneously reducing the complexity of the decoders. Similar coding gains and complexity reductions would be the focus of the proposed effort when there is an additional constraint on bandwidth efficiency. These investigations would rely on the use of linear bandwidth efficient modulations (e.g., pulse-shaping and higher order modulations) and the results would serve to recoup some of the power efficiency loss associated with employing such modulations. Decoder complexities would be evaluated through comparison with decoders for conventional codes. (2) Turbo coded CPM research - This represents a completely new concept in combining modulation and coding based upon the turbo-coding concept, which combines simple constituent codes. In this technique, one of the codes will be represented by the memory in the CPM waveform. This technique is similarly applicable to filtered signals that exhibit intersymbol interference. From a system perspective, CPM is less susceptible to the vagaries and impairments of non-linear transmitter amplification (e.g., saturated TWTAs or SSPAs) than are linear pulse shaped waveforms and/or higher order linear modulations. These investigations are directed towards developing the correct methodology to add low-complexity, high coding gain capability to a waveform that is inherently suitable for non-linear transmitters. (3) Very High Speed Digital Demodulator and Decoder Design - Advanced high-speed demodulator/decoder technologies will be examined by merging the coding technology developments by JPL with the multi Gbps

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<sup>1</sup> In fact CPM modulation can be viewed as a similar combination of spectral coding and memoryless modulation, which guarantees the constant envelope property.

hardware design expertise by TRW.

#### 2.4.1 Conventional Bandwidth Efficient Modulation Techniques.

An appropriate point of departure for the proposed research is a thorough investigation and evaluation of well-known bandwidth efficient modulation techniques<sup>2</sup> [2][3] for the non-linear channel. This will form a baseline for comparison of novel coded modulation schemes developed in this task.

Depending upon the communication engineer's priorities, trellis coded modulation (TCM) or continuous phase modulation (CPM) with coding may represent an attractive choice for the system design. A number of significant issues will begin to obscure the relative advantages of one selection over another when migrating to the high-speed environment. These may include frequency selective linear and non-linear signal distortions requiring appropriate mitigation strategies. These include the examination of pre-coding benefits, equalization for reduction of unintentional intersymbol interference and decoder modifications to account for memoryless non-linearities in the form of AM-to-AM and AM-to-PM distortion. Both these and subsequent evaluations of novel techniques will employ non-linear channel models developed under a system overview element of this task.

#### 2.4.2 Near-term Modulation and Coding Solutions.

Turbo codes [4] represent a quantum leap in channel coding performance, providing higher coding gain and much lower decoding complexity than current advanced coding systems (See Fig. 1). JPL has advanced the state-of-the art in channel coding for applications such as deep space communications where the highest possible power efficiency is required.

**Turbo Trellis Coded Modulation (TTTCM).** The extension of turbo codes [4] to turbo coded modulation schemes for bandwidth efficiency was first proposed by JPL [9] (a patent is pending for this concept). This approach to high power/bandwidth efficiency is already under study at JPL. Current results indicate that we can develop codes within 1 dB from channel capacity at 2 to 4 bits/sec/Hz spectral efficiency. Shaded regions in Fig. 2 are possible throughput/power operating conditions for proposed telecom systems. The challenge here is to find even better performing turbo codes, which typically can achieve lower bit error rates. These codes must have low complexity so that a high-speed iterative decoder [7] can be developed. A feasibility study will include the definition of the high-speed decoder architecture. In the following two design examples, we illustrate the operation of the TTTCM concept.

*Parallel Concatenated Trellis Coded Modulation (PCTCM).* The basic structure of parallel concatenated trellis coded modulation is shown in Fig. 3. This structure uses two rate  $2b/(2b+1)$  constituent systematic recursive convolutional codes. The first  $b$  most significant output bits of each convolutional code are only connected to the shift register of the TCM encoder and are not mapped to the modulation signals. The last  $b+1$  least significant output bits however are mapped to the modulation signals.

This method requires at least two interleavers (the combined interleavers are shown as one interleaver in Fig. 3). The first interleaver permutes the  $b$  least significant input bits. This interleaver is connected to the  $b$  most significant bits of the second TCM encoder. The second interleaver permutes the  $b$  most significant input bits. This interleaver is then connected to the  $b$  least significant bits of the second TCM encoder.

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<sup>2</sup> Extensive research and development on conventional TCM systems was done at JPL in the 1980s and beginning of 90s [2].

The  $b+1$  output bits of each encoder are mapped to one of  $2^{(1+b)}$  modulation levels. The throughput of the described encoding scheme is  $b$  bits per symbol duration for a  $2^{(b+1)}$  point modulation or  $b$  bits/sec/Hz if an ideal Nyquist filter is used.

*Example:* For  $b=2$  (bps/Hz) using two parallel 16-state convolutional codes with 8PSK modulation we achieved a bit error rate of  $10^{-6}$  at  $E_b/N_0=3.6$  dB for input block of 16384 bits using the iterative decoder with soft-in soft-out (SISO) modules [7] shown in Fig. 4 with 8 iterations. This is 0.8 dB from Shannon's limit with infinite block size and infinite complexity.

*Serial Concatenated Trellis Coded Modulation (SCTCM).* We extend serial concatenated codes, developed in [6] for binary modulations, to higher order modulations. The basic structure of serially concatenated trellis coded modulation is shown in Fig. 5. We propose a novel method to design serial concatenated TCM, which achieves  $b$  bits/sec/Hz, using a rate  $2b/(2b+1)$  binary convolutional encoder, with maximum free Hamming distance, as the outer code. We interleave the output of the outer code with an interleaver  $\pi$ . The interleaved data enters a rate  $(2b+1)/(2b+2)$  recursive convolutional inner encoder. The  $2b+2$  output bits are mapped to two symbols each belonging to a  $2^{b+1}$  level modulation (four-dimensional modulation). In this way, we are using  $2b$  information bits for every two modulation symbol intervals, resulting in  $b$  bit/sec/Hz transmission (when ideal Nyquist pulse shaping is used) or, in other words,  $b$  bits per modulation symbol. The inner code and the mapping will be jointly optimized based on maximizing the effective free Euclidean distance of the inner TCM. In the serial case, however, the inputs to the inner code are not unconstrained bits as in the PCTCM, and thus the design methodology must be different.

*Example:* For  $b=2$  (bps/Hz) using an 8-state, rate  $4/5$  convolutional code (this code can be obtained by puncturing a rate  $1/2$  code) and a 2-state TCM, we can achieve bit error rate of  $10^{-7}$  at  $E_b/N_0=3.7$  dB for 16384 bit interleaver with 8-iterations, using the decoder shown in Fig. 6. Results of several examples are summarized in Fig. 7. To achieve the bandwidth efficiency shown in Fig. 7, ideal Nyquist pulse shaping with no excess bandwidth is assumed.

### 2.4.3 Advanced Combined Modulation and Coding Solutions.

**Parallel Architecture for SCTCM.** The basic parallel structure that is being proposed for SCTCM is shown in Fig. 8 for the specific case of 8 PSK. This structure is also applicable to general  $M$ -level modulations. For  $M$  level modulations such as  $M$ -PSK (example 8-PSK) or  $M$ -QAM (example 16-QAM), data at rate  $R$  is de-multiplexed into  $(\log_2 M)$  streams each with data rate  $R/(\log_2 M)$ . So for each stream the data rate is decreased by factor of  $(\log_2 M)$ . For example: for 8-PSK by factor of 3, and for 16QAM by factor of 4. Now each data stream is encoded by a very low complexity convolutional code (for example a 4-state code). The encoded data are interleaved and enter another very low complexity recursive convolutional code (for example 2-state). These component convolutional codes, used in the examples, are *binary* codes<sup>3</sup> and they are less complex than the 64-state NASA-standard convolutional code by factors of 16 and 32, respectively. The outputs of overall encoded streams are then mapped to  $M$  level modulation. The iterative turbo decoder, also consisting of *binary* component decoders, is shown in Fig. 9. The parallel binary turbo-like encoders are matched to the modulation through appropriate mapping. Similarly, the component binary decoders are matched to the demodulator according to the bit reliability generator outputs. The advantage of the proposed parallel architecture is that each binary encoder and decoder operates at  $1/3$  of the actual data rate for 8 PSK, at  $1/4$  for 16QAM, or at  $1/5$  for 32QAM. Therefore, this architecture enables the implementation of the overall system at high data rates, while the components need to operate only at much lower data rates.

<sup>3</sup> The proposed parallel architecture offers a unique advantage of using simple *binary* codes. A patent application for this technique is in progress.

**Turbo Coded CPM.** In this task, we also propose to concatenate convolutional codes with CPM with an interleaver (turbo CPM) for cases strictly requiring constant envelope modulation. A turbo CPM scheme with iterative decoding is superior in terms of complexity and performance to conventional coded CPM, where a convolutional code is combined directly with CPM and a high-complexity Viterbi decoder is needed. The promise of this approach is the coupling of a non-linearity tolerant waveform (CPM due to its constant envelope) with a low complexity convolutional encoder to achieve turbo code type gains.

Turbo codes (concatenated codes with interleavers) with iterative decoding can perform close to channel capacity with reasonable decoding complexity. They are the most powerful codes with a practical low complexity decoder. Most known turbo codes have been designed for memoryless channels. In many practical applications, including satellite communications requiring very high data rates, the use of CPM is desirable to conserve bandwidth, e.g., quaternary CPM with optimized filtering outperforms MSK (Minimum Shift Keying) by 3.5 dB and also reduces the 30-dB bandwidth by 20%). CPM provides both resistance to non-linearities (power transmitter) by its inherent constant amplitude transmission and very compact spectrum for bandwidth efficiency.

Spectral efficiency is achieved by partial response signaling which generates (non-linear) dependencies between successive symbols. CPM (which is a non-linear modulation with memory) can be described through a trellis diagram (hence can be viewed as a trellis code). This trellis code by itself is quite weak. However, in a turbo code structure the weakness of constituent codes is compensated by the coupling with other constituent codes through interleavers, so that the overall code can be much stronger.

To enjoy the benefits of CPM, optimum coherent detection should be used. Conventional carrier tracking methods need to generate discrete spectral components for  $M$ -phase CPM, which require the signal to be raised to the  $M$ th power. We propose to address this issue with an advanced scheme based on a coupled demodulator/decoder concept.

*Design of turbo coded CPM.* Turbo coded CPM can be designed in many ways. The simplest scheme can be viewed as serial concatenation of a convolutional or simple short block code (as an outer code), an interleaver, and CPM modulation (as an inner code), as shown in Fig. 10. CPM, which inherently has memory, can be decomposed into two components. The first component can be modeled as a discrete time encoder, and the second component can be modeled as a memoryless modulator that takes the encoded symbols from the first component and maps to waveforms with one symbol duration. The CPM decomposition is not required to implement the transmitter. However this decomposition is required to define: 1) the structure of demodulator (matched to the second component in the decomposition) and 2) the structure of inner decoder (matched to the first component in the decomposition). The structure of the iterative decoder for turbo CPM will be similar to that in Fig. 6.

*Example - Turbo Coded MSK.* In this example (valid only for low throughput) we show our design methodology by considering MSK which is a special case of CPM. MSK is full response binary CPM with rectangular frequency pulse shape and modulation index of 0.5. Turbo coded MSK is shown in Fig. 11. The power spectral density of MSK is shown in Figure 10. MSK can be decomposed into two component as shown in Figure 11.

This decomposition guides us to obtain: 1) the structure of the soft output demodulator, which consists of matched filters. 2) the structure of the 2-state decoder which is matched to the 2-state encoder in the decomposition of MSK.

The performance of the iterative decoder of Figure 12 is shown in Figure 13 for 1024 bit input block size for 4 and 10 iterations. Larger block sizes results in a better performance. The main points that this example illustrates are: (1) The design method to be used for turbo CPM. (2) That the iterative decoder is based on two simple 2-state and 4-state decoder modules which implies a

very low complexity system for high data rates. (3) For this simple structure for 4 iterations we obtain an excellent performance gain of 8 dB with respect to uncoded MSK and 2 dB with respect to the slightly higher complexity 64-state Viterbi decoder for a bit error rate of  $10^{-6}$ . We expect to achieve similar gains for high throughput applications by using higher level CPM modulations with high rate outer codes.

#### 2.4.4 Digital Modulator/Demodulator and Decoder Architectures

The research effort described in this section will investigate the signal processing architectures necessary to support very high data rate communications in conjunction with newly proposed coded modulation schemes. The specific objective of this part of the task is to determine realistic hardware implementations and a roadmap for technology infusion, final fabrication, and collaboration with industry.

**High-Speed Digital Demodulators.** The first area (modulator/demodulator) leverages on the extensive expertise offered by TRW in high-speed communication hardware. TRW has a 20 year-plus history in producing high-rate communication equipment for NASA and government projects, and has a thorough understanding of the challenges posed by high-speed hardware for space communications. TRW will evaluate hardware implementations for the proposed advanced modulation and coding techniques.

Parallel algorithms for the demodulator will take advantage of frequency domain processing rather than the traditional time domain approach. These parallel algorithms will be jointly developed by JPL and TRW.

The modulator and demodulator will be designed for future implementation in 1 micron GaAs digital ICs. The basis for this design will be the TRW modulator shown in Fig. 16, which was developed for R&D purposes. This modulator is capable of multiple modulation techniques with a maximum rate of 12.0 Gbps when transmitting 32QAM at 2.4 Gbps. (It is also capable of producing QPSK, 8PSK, and 16QAM). This design will be modified to incorporate the proposed modulations and to include the encoders. This technology will also be the basis for the demodulator design. We envision speeds well in excess of 1 Gbps.

**High-speed turbo decoders.** The second area (decoder) will examine decoder architectures, which are specialized for the proposed low-complexity codes. It will define suitable parallel architectures (See Fig. 9 for example), and investigate simplified decoding rules. These decoder architectures will be evaluated by TRW for hardware implementation at very high speed.

We will approach the problem of designing high speed turbo decoders based on reducing the code complexity while maintaining a coding gain better than is possible with current (non-turbo) codes.

#### 2.4.5 System Overview and Channel Modeling

A system level consideration of the potential benefits provided through enhancements in modulation, coding and signal processing is a necessary adjunct to the research performed under this project. The charter of this oversight is to simply insure that all solutions are compared in an equivalent fashion from the standpoint of system resources (e.g., DC power consumption of an amplifier operating at varying levels of back-off). In addition, realistic channel modeling of the frequency selective filtering and non-linear effects will be used in the final evaluation of any proposed solutions. It is envisioned that representative test data from commercial components, such as TWTAs or SSPAs would be incorporated into these models. If suitable, a meaningful metric or cost function will be developed to account for varying emphases on power, bandwidth or processing complexity.

## **2.5 Relevance of the Proposed Work**

This proposal directly addresses the needs of the “High Data Rate Delivery” thrust (NRA proposal call, Section A4, bullet #6). The proposed technology development will significantly benefit a number of future projects in the Earth and Space Science domain, which require high data rate transmission from spacecraft to ground at X or Ka-band. Data rates generated by on-board instruments are continually increasing, putting severe requirements on the communication link, together with the necessity for smaller and more efficient transmission systems.

For example the NMP EO-1 mission has an “Advanced Land Imager” instrument generating multispectral and hyperspectral data at 383 Mbps; Multispectral data rates from Landsat 7 can reach 135 Mbps. Future mission demands in terms of data rates will be even higher, reaching the Gbps domain at Ka-band. The proposed techniques will enable these high data rate links within ever more stringent RF spectrum allocations and reduce the transmission power required.

Mars exploration will require high data rates for live video coverage and for virtual reality projects.

The Space Science Enterprise and Earth Science Enterprise will greatly benefit from the availability of power and bandwidth efficient communication links. The proposed technology will reduce the required transmitter power (hence mass and size) and/or increase the data throughput.

The anticipated advantages of the proposed techniques are a reduction of the required transmitter power on the satellite, at least 2 dB improvement over the current state-of-the-art, and the availability of a bandwidth efficient transmission system, which can be implemented at very high data rates, due to advances in low-complexity, high performance codes, and in parallel architectures for decoders and receivers.

Ultimately, the proposed new technologies will enable spacecraft to ground transmission of data with smaller spacecraft and at data rates up to and above 1 Gbps.

## **2.6 Management Plan**

In order to maximize the benefits of the research suggested in this proposal, the organization of the work has been structured at several different levels of technology risk. These range from delivery of a comprehensive evaluation of current conventional techniques, to the development of a theoretically based methodology for the concatenated combination of low complexity codes and high level modulations. It is expected that this distribution of risk will be sufficient to deliver a broad spectrum of technology products that span incremental to revolutionary improvement in communications systems design.

The proposed technology developments are currently at TRL 1 to 2, depending on the specific subtask. This effort will bring all the proposed technology items to at least TRL 3, and will be the basis for fast infusion of new technology on operational communication subsystems, by indicating the optimal path for hardware implementation.

JPL will evaluate, research and develop current and new technologies to be applied to high data rate, bandwidth and power constrained, spacecraft to ground communications. These technologies will include turbo code designs, turbo decoder structures and parallel demodulator architectures. JPL will, on a best effort basis, deliver the following products and reports, in collaboration with TRW.

### **2.6.1 Deliverables and Schedule**

This schedule provides a timeline of the expected progress in each of the identified subtasks (A to M). Milestone dates are measured in months elapsed from the beginning of the task, up to 36 months.

- A. Perform an in-depth survey of state-of-the-art modulation and coding for bandwidth efficient communications on non-linear channels.
- B. Form a baseline for later comparisons.

Turbo trellis coded modulation:

- C. Comprehensive code designs (Parallel and serial concatenated TCM).
- D. Performance evaluations through simulation and bounds for the linear channel.
- E. Performance evaluations through simulation or analysis for the non-linear channel.

Turbo coded CPM research:

- F. A formulation of the fundamental approaches to turbo coded modulation design.
- G. Designs of coded modulations suitable for high-speed, high-throughput satellite to ground communications.
- H. Performance evaluations through simulation.

High speed demodulator and decoder architectures:

- I. Parallel demodulator extensions to accommodate detection and equalization of higher order modulations.
- J. Turbo decoder architectures.
- K. System-level overview, comparisons, and tradeoffs: final report.

Additional documentation of this work will be in the form of the quarterly reports, interim and annual reviews, annual reports, and papers submitted to appropriate conferences and journals.

The proposed work will consist of the following subtasks:

MILESTONE	YEAR 1	YEAR 2	YEAR 3
Quarterly review	▲	▲	▲
Annual reports	▲	▲	▲
Final report			▲
A	→		
B	→		
C		→	
D		→	
E		→	
F		→	
G		→	
H		→	
I			→
J			→
K			→

## 2.7 Expected Contribution

D. Divsalar will be responsible for the development of new coded modulation schemes and for their analysis. He will also oversee the overall performance of all the proposed subtasks. K. Andrews will support this development work and implement a software simulation infrastructure that will be used to compare new schemes to current state-of-the-art and to analyze tradeoffs. F. Pollara will collaborate in all the above activities and be responsible for oral and written reports. S. Dolinar will be responsible for the planned system-level overview and related tradeoffs. He will also contribute to the final report preparation. R. McEliece will provide unique expertise in the theoretical aspects related to analytical performance evaluation. C.W. Walker will collaborate in the definition of high-speed demodulator and decoder architectures and evaluate their feasibility with advanced technology available at TRW.

### 3 Figures

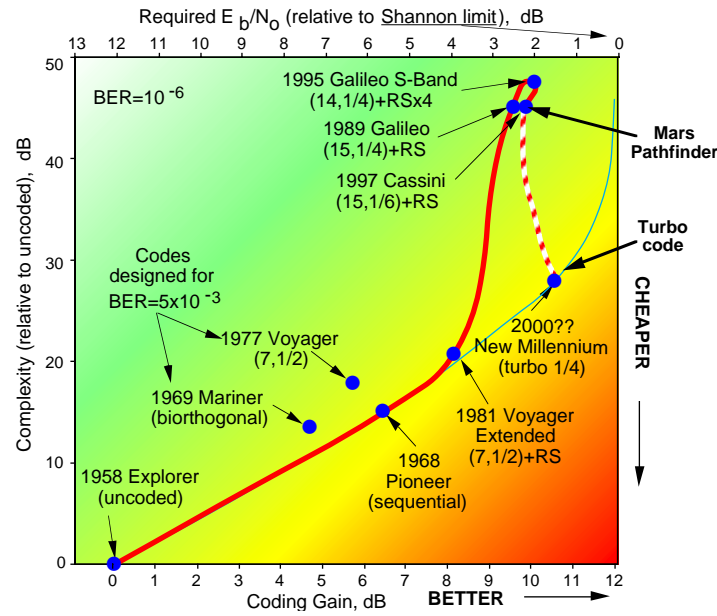


Figure 1 - Performance/complexity of coded systems for deep space missions

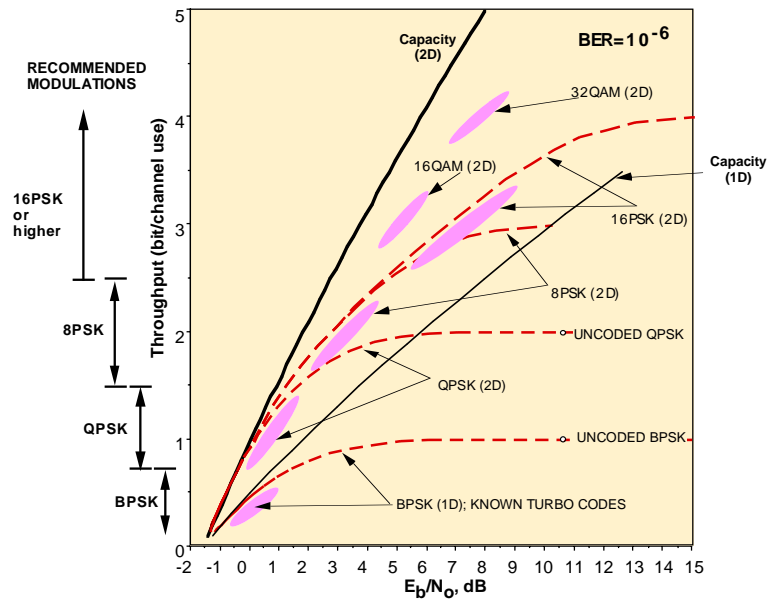
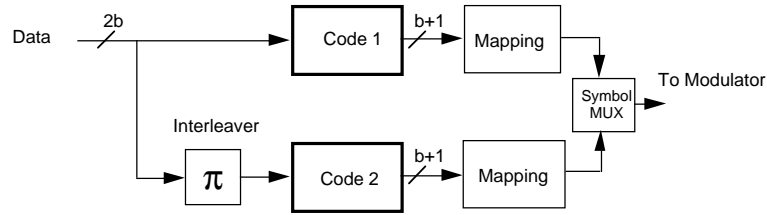
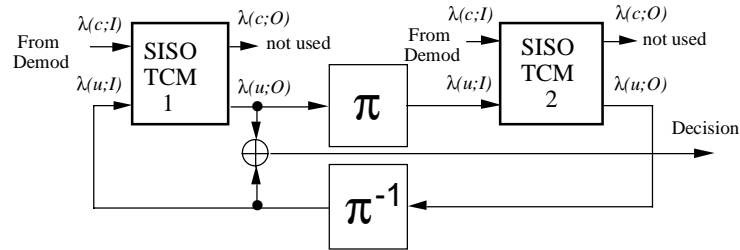


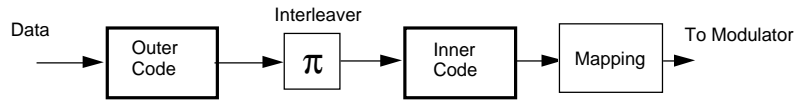
Figure 2 - Power and bandwidth efficiency of projected TTCM systems



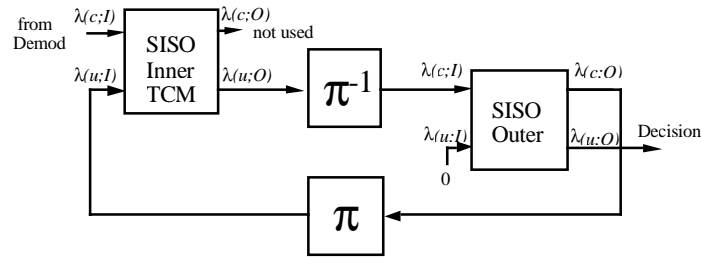
**Figure 3 - Parallel concatenated TCM**



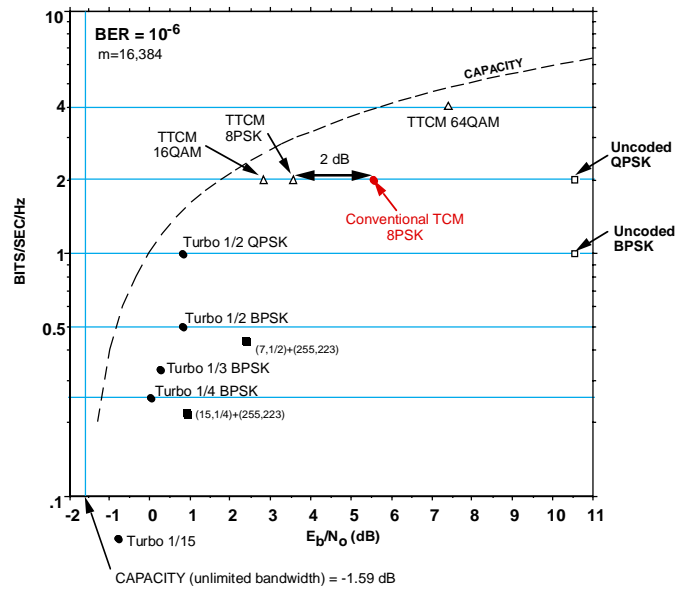
**Figure 4 - Iterative decoding of parallel concatenated TCM**



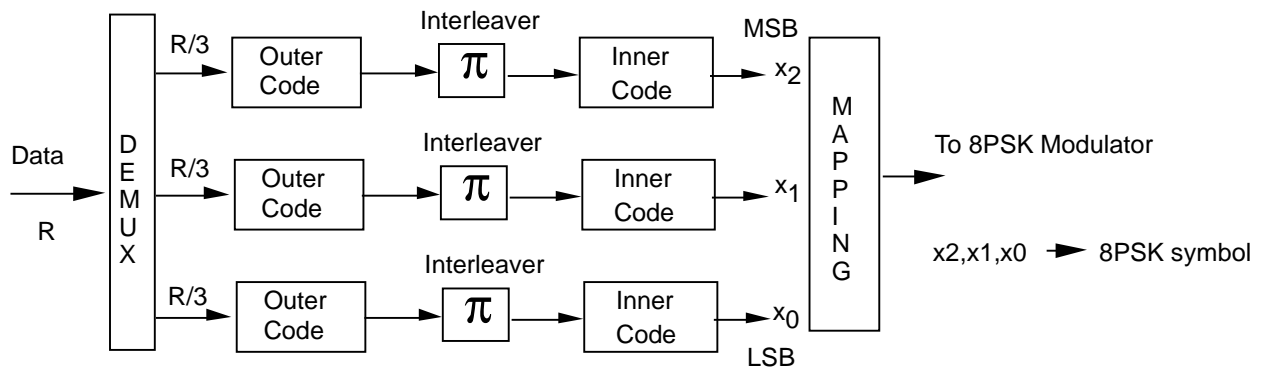
**Figure 5 - Serial concatenated TCM**



**Figure 6 - Iterative decoding of serial concatenated TCM**



**Figure 7 - Performance of TTCM**



**Figure 8 - Parallel architecture for SCTCM encoder**

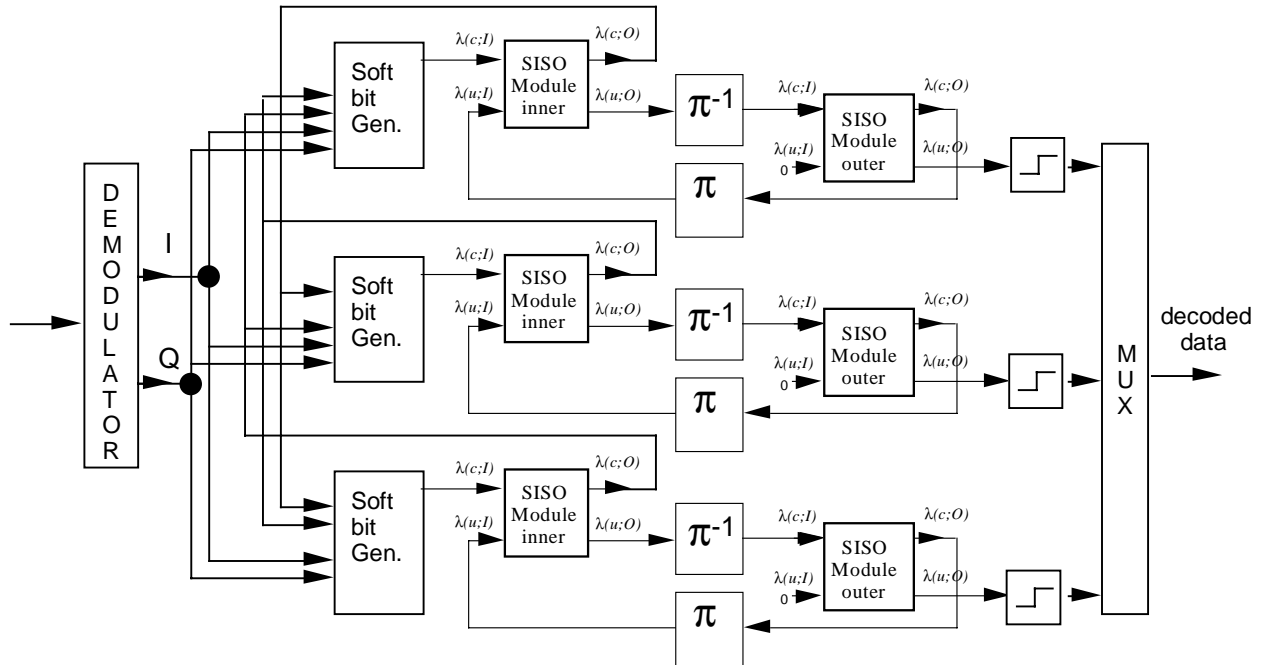


Figure 9 - Parallel architecture for SCTCM decoder

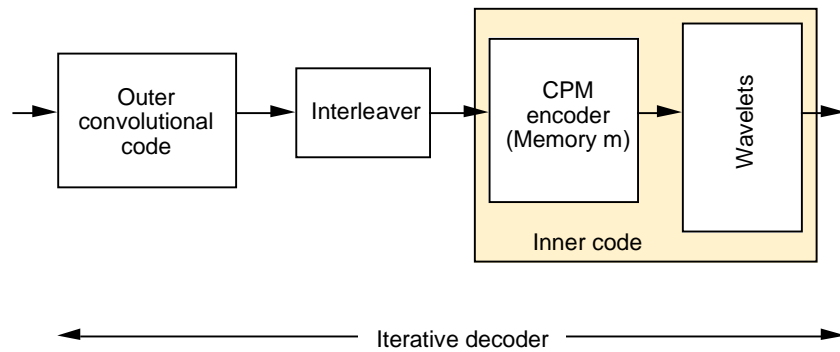


Figure 10 - Turbo CPM

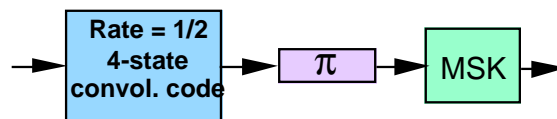


Figure 11 - Turbo coded MSK

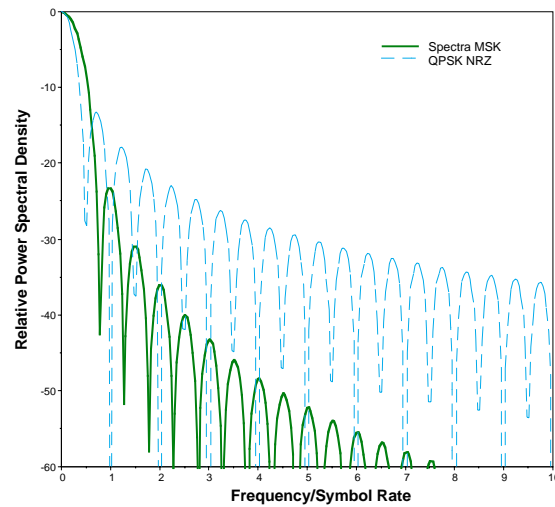


Figure 12 - Spectra of MSK

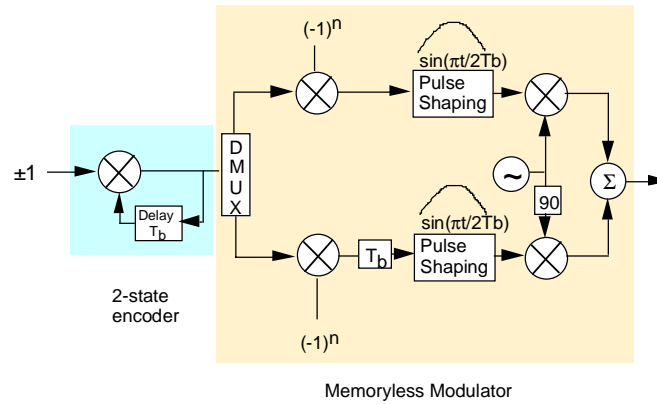


Figure 13 - Decomposition of MSK

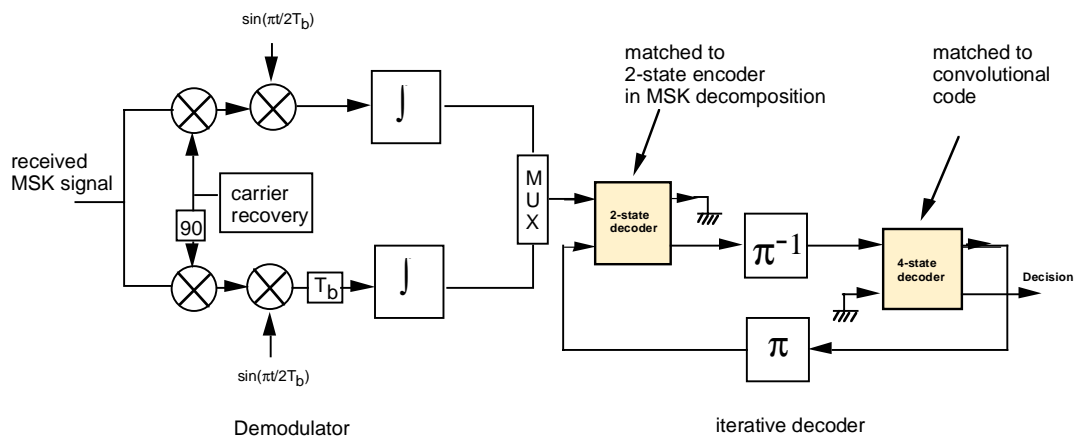
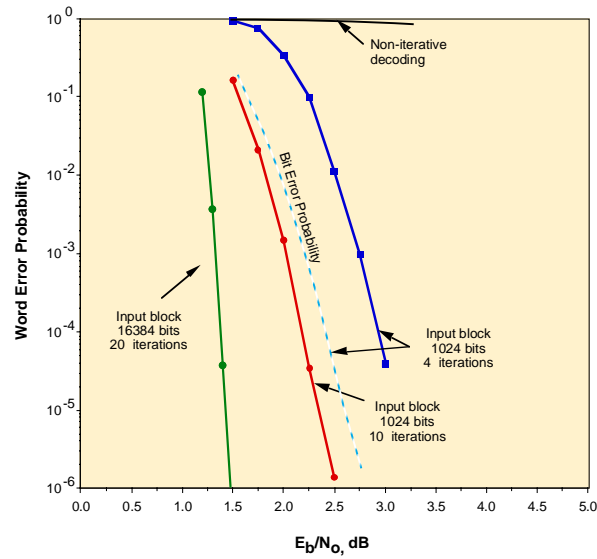
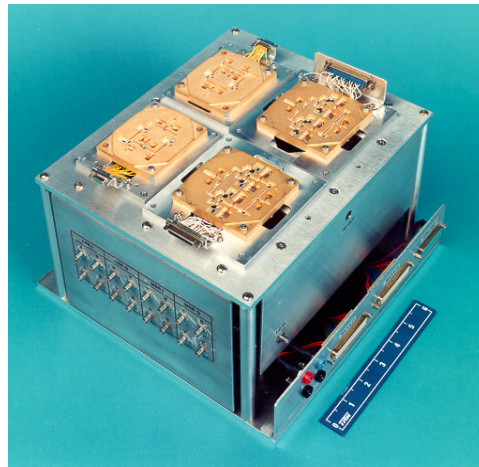


Figure 14 - Demodulator and Iterative decoder for coded MSK



**Figure 15 - Performance of convolutional code and MSK modulation with iterative decoding**



**Figure 16 - 2.4 Gbps TRW modulator: QPSK, 8PSK, 16QAM and 32QAM (12 Gbps with 32QAM)**

## 4 References

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- [2] E. Biglieri, D. Divsalar, P. McLane, M. Simon, "Introduction to Trellis-Coded Modulation with Applications", MacMillan 1991.
- [3] G. Ungerboeck, "Channel coding with multilevel phase signaling", IEEE Trans. Inf. Th., vol. IT-25, pp.55-67, Jan. 1982.
- [4] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon Limit Error-Correcting Coding: Turbo Codes," Proc. 1993 IEEE International Conference on Communications, Geneva, Switzerland, pp. 1064--1070, May 1993.

- [5] D. Divsalar, F. Pollara, "On the Design of Turbo Codes", JPL TMO Progress Report 42-123, Nov 15, 1995,
- [6] S. Benedetto, D. Divsalar, G. Montorsi, F. Pollara, "Serial concatenation of interleaved codes: performance analysis, design, and iterative decoding", Information Theory, IEEE Transactions on, Volume: 44, May 1998, Page(s): 909 -926.
- [7] S. Benedetto, D. Divsalar, G. Montorsi, F. Pollara, "Soft input soft output MAP module to decoded parallel and serial concatenated codes," JPL TMO Prog. Report, Nov. 15, 1996.
- [8] S. Benedetto, D. Divsalar, G. Montorsi, F. Pollara, "Serial Concatenated Trellis Coded Modulation with Iterative Decoding: Design and Performance," IEEE Global Telecommunications Conference, (CTMC), November 1997.
- [9] D. Divsalar, F. Pollara, "Turbo Trellis Coded Modulation with Iterative Decoding for Mobile Satellite Communications", International Mobile Satellite Conference, June 1997.

## **5 Facilities and Equipment**

JPL maintains state-of-the-art networked computing facilities, which are sufficient for the simulation and computer-aided development of the proposed technology items. The only new software tool that may be required for this task is an additional license for the Signal Processing Workstation (SPW) software package or its use on the JPL-maintained Design Hub facility. TRW has extensive facilities and equipment for the design, evaluation, and testing of high-speed communication subsystems and components. TRW will be the conduit for future fabrication of the codec with state-of-the-art GaAs technology.

## 6 Biographies

*Dariusz Divsalar.* Senior Scientist in the Communications Systems and Research Section, JPL, Pasadena, received M.S., Engineer, and Ph.D. degrees all in Electrical Engineering from UCLA, in 1975, 1977, and 1978 respectively. He joined JPL in October 1978. Since that time, he has been working on developing state-of-the-art technology for advanced deep space communications systems. He has contributed to many research and advanced projects including: VOIR, Venus Balloon, Antenna Arraying, Galileo, ICE, LMSS, MSAT-X, TDA Advanced Systems RTOP's on optical communication, Galileo S-band, NASA ACTS Mobile Terminal (AMT), JPL-FAA Helicopter. His areas of interest are coding, digital modulation, and in particular turbo codes. During the last twelve years, he has taught electrical engineering courses and short courses at UCLA and recently at Caltech. He has published over 120 technical papers, and holds six U.S. patents in related areas. Dr. Divsalar received over 20 NASA Tech Brief awards and a NASA Exceptional Engineering Achievement Medal in 1996. He is a Fellow of the Institute of Electrical and Electronics Engineers.

### Relevant Publications:

- Divsalar, F. Pollara, "On the Design of Turbo Codes", JPL TMO Progress Report 42-123, Nov 15, 1995,
- S. Benedetto, D. Divsalar, G. Montorsi, F. Pollara, "Parallel concatenated trellis coded modulation". Conference Record, 1996 IEEE International Conference on Communications Volume: 2, 1996 , Page(s): 974 -978 vol.2
- S. Benedetto, D. Divsalar, G. Montorsi, F. Pollara, "Serial concatenation of interleaved codes: performance analysis, design, and iterative decoding". Information Theory, IEEE Transactions on Volume: 44 3 , May 1998 , Page(s): 909 -926
- S. Benedetto, D. Divsalar, G. Montorsi, F. Pollara, "Soft input soft output MAP module to decode parallel and serial concatenated codes", JPL TMO Prog. Report, Nov. 15, 1996,
- Benedetto, Divsalar, Montorsi, Pollara, "Serial Concatenated Trellis Coded Modulation with Iterative Decoding: Design and Performance," IEEE Global Telecommunications Conference, (CTMC), November 1997.
- Divsalar, F. Pollara, "Turbo Codes for Deep-Space Communications", JPL TMO Progress Report 42-120, Feb. 15, 1995.
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- Divsalar, D.; Pollara, F., "Hybrid Concatenated Codes and Iterative Decoding", JPL TMO Prog. Report, Aug. 15, 1997.
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- S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, "A Soft-Input Soft-Output APP Module for Iterative Decoding of Concatenated Codes," IEEE Communications Letters, vol.1, no.1, January 1997.
- S. Benedetto, D. Divsalar, G. Montorsi, F. Pollara, "Iterative decoding of serially concatenated codes with interleavers and comparison with turbo codes", Global Telecommunications Conference, 1997. GLOBECOM '97, IEEE, Volume: 2 , 1997 , Page(s): 654 -658 vol.2
- S. Benedetto, D. Divsalar, G. Montorsi, F. Pollara, "Analysis, design, and iterative decoding of double serially concatenated codes with interleavers", Selected Areas in Communications, IEEE Journal on Volume: 16 2 , Feb. 1998 , Page(s): 231 -244
- S. Benedetto, D. Divsalar, R. Garelo, G. Montorsi, F. Pollara, "Bit geometrically uniform encoder and applications to serially concatenated trellis coded modulation Information Theory, 1998. Proceedings. 1998 IEEE International Symposium on , 1998, Page(s): 175

- S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, "Serial Concatenated Trellis Coded Modulation with Iterative Decoding: Design and Performance," IEEE Global Telecommunications Conference, (CTMC), November 1997.
- S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, "Serial Concatenated Trellis Coded Modulation with Iterative Decoding", IEEE International Symposium on Information Theory 97, Germany July 1997.

*Fabrizio Pollara* is a Technical Group Supervisor in the Communications Systems and Research Section, Jet Propulsion Laboratory, Pasadena. He manages source and channel coding research for NASA's Deep Space Network technology program. He received a MS degree (1977) and a Ph.D. degree (1982) in Electrical Engineering from the University of California, Los Angeles. Since 1983 he has been with JPL, where he contributes to the development of advanced communication systems for deep space missions. Research work includes development of new error-correcting coding systems, including concatenated codes and iterative decoding methods. His early work on parallel decoding algorithms has contributed to the development of the decoders for very large constraint length convolutional codes that are now used for deep space NASA missions. He has been teaching error-correction coding theory as a part-time Lecturer in the Electrical Engineering department at the California Institute of Technology. He has published over 50 technical papers, and was granted two U.S. patents and several NASA certificates of recognition.

*Kenneth Andrews* is a member of the Communications Systems and Research Section, Jet Propulsion Laboratory, Pasadena. He received the B.S. degree in Applied Physics from Caltech in 1990, and Ph.D. degree in Electrical Engineering from Cornell in 1999. From 1990-1994, he worked at Altadena Instruments, Pasadena, on spacecraft cameras for the Mars Observer and Mars Global Surveyor missions. His current research work is in error correcting codes and decoder implementations.

*Samuel Dolinar*, Member of the Technical Staff in the Communications Systems Research Section, received S.B., S.M., E.E., and Ph.D. degrees from the Massachusetts Institute of Technology. He came to JPL in 1980 after four years at MIT Lincoln Laboratory, where he worked on problems in direction finding and multipath analysis with applications in aviation systems. At JPL, Dr. Dolinar initially worked on deep-space optical communication systems, electronic warfare software, and tactical communication systems. During the past fourteen years, his work has focused on channel coding and source coding for the deep-space channel. Dr. Dolinar led the search for Galileo's experimental long constraint length code, made original contributions to the DSN Viterbi decoder development, and studied the effect of data gaps in the Very Large Array (VLA) on code performance. For four years in the early 1990's he was a co-organizer of the NASA Space and Earth Science Data Compression Workshop. He has helped to develop improved bounds on the performance of linear block codes and on the complexity of trellis structures used for soft-decoding them. He analyzed and guided the development of the iterative decoding scheme used by the Galileo mission to salvage sufficient coding performance while operating with the low-gain antenna. During the past five years, his work has focused on turbo codes and turbo-like codes, and their associated iterative decoding algorithms. He has developed theoretical bounds on the performance of such codes and shown how closely this performance approaches that of the best possible codes of the same block sizes. Last year he also taught a graduate-level course on Data Compression as a part-time Lecturer in the Electrical Engineering department at the California Institute of Technology.

*Robert J. McEliece* is the Allen E. Puckett Professor of Electrical Engineering at the California Institute of Technology. He received the B.S. and Ph.D. degrees in mathematics at Caltech in

1964 and 1967, respectively. From 1963--1978 he was employed at the Jet Propulsion Laboratory, where he worked in the Information Processing Group of the Communications Systems and Research Section. From 1978--1982 he was a Professor of Mathematics and Research Professor at the Coordinated Science Laboratory at the University of Illinois, Urbana-Champaign. He joined the faculty at Caltech in 1982, and has served as Executive Officer (department chair) for Electrical Engineering since 1990. He has published over 200 scientific papers, is a member of the American Mathematical Society, a Fellow of the Institute of Electrical and Electronics Engineers, and a member of the National Academy of Engineering.

*Christopher Wayne Walker* is currently a member of the Senior Engineering Staff in the Systems Engineering Integration and Test Center at TRW in Redondo Beach, CA where he has been employed for the last 12 years. Prior to that he worked at Scientific-Atlanta, Georgia Tech Research Institute, Texas Instruments and the Tennessee Valley Authority. Dr. Walker works primarily in the areas of communications, signal processing and coding theory. He holds a Ph.D. in Electrical Engineering from the University of Southern California where he studied coding theory under the direction of Professor Solomon Golomb. He also earned a Master of Science degree in Applied Mathematics and a Master of Arts degree in Mathematics all from USC. Dr. Walker also teaches occasionally at USC (probability theory and random processes), UCLA (digital signal processing) and Santa Monica College (mathematics). He has presented research at conferences and has published in the IEEE Transactions on Information Theory.

## **7 Current and Pending Support**

Divsalar, Pollara, Andrews, and Dolinar are partially supported in FY00 by the “TMOD Technology Program” at JPL. Funding commitments for future years are currently not available. The investigators plan to actively pursue research opportunities at NASA and other agencies. There are no pending funds that have been already awarded.

McEliece is a professor at the California Institute of Technology, and Walker is a senior member of technical staff for communication technology at TRW. They have no pending NASA funds that have been already awarded.

## **8 Compliance with NRA Guidelines**

This proposal directly addresses the needs of the “High Data Rate Delivery” thrust (NRA proposal call, Section A4, bullet #6: “Efficient, high data rate modulation, coding, and signal processing/switching technologies and components for enhanced data throughput”). The proposed technology development will significantly benefit a number of future projects in the Earth and Space Science Enterprises, which require efficient, high data rate transmission.

The intrinsic technical value of this proposal is in the development of revolutionary, advanced coding/modulation technologies, which can save power and bandwidth and can operate at very high data rates. Dramatic improvements in mission design will be possible by applying the innovative and unique concepts here proposed along with a roadmap for their development and future implementation.

The potential impact of the proposed technology has a wide breadth of applicability to the three main NASA Enterprises and to additional commercial and defense related advanced projects.

The personnel involved have outstanding academic, research, and industrial qualifications, including two IEEE fellows, a JPL senior scientist, and a member of the National Academy of Engineering. This research group has a history of outstanding contributions to the theory and practice of coding and modulation, and is well-known worldwide for its unique achievements.

All the above ingredients are a guarantee that the proposed effort will advance the state-of-the-art. Furthermore this will obtain significant cost benefits in a number of future missions, thus greatly multiplying the investment of this research effort.

## 9 Co-I and Collaborator Letters of Commitment.

Jet Propulsion Laboratory  
California Institute of Technology  
4800 Oak Grove Drive  
Pasadena, California 91109-8099  
(818) 354-4321



January 12, 2000

Dariusz Divsalar  
Jet Propulsion Laboratory  
California Institute of Technology  
M/S 238-420  
4800 Oak Grove Drive  
Pasadena, CA 91109-8099

Dear Dr. Divsalar,

We acknowledge that we are identified by name as Co-Investigators to the investigation entitled "Power and Bandwidth Efficient Coded Modulation for Very High Data Rates," that is submitted by Dr. Dariusz Divsalar to the NASA Research Announcement 99-OSS-05 and that we intend to carry out all responsibilities identified for us in this proposal.

Sincerely

Fabrizio Pollara

Handwritten signature of Fabrizio Pollara in black ink.

Kenneth Andrews

Handwritten signature of Kenneth Andrews in black ink.

Samuel Dolinar

Handwritten signature of Samuel Dolinar in black ink.

CALIFORNIA INSTITUTE OF TECHNOLOGY

ELECTRICAL ENGINEERING 136-93

Robert J. McEliece  
Allen E. Puckett Professor

(626)395-3891  
FAX (626)564-9307

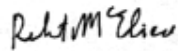
January 14, 2000

TO WHOM IT MAY CONCERN

**Re: 632 NRA Proposal**

I acknowledge that I am identified by name as a Co-Investigator to the investigation entitled "Power and Bandwidth Efficient Coded Modulation for Very High Data Rates, that is submitted by Dr. Dariush Divsalar to the NASA Research Announcement 99-OSS-O5. I also acknowledge that I intend to carry out all responsibilities identified for me in this proposal.

Sincerely,



Robert J. McEliece

RJM/lp

PASADENA, CALIFORNIA 91125



**TRW Telecommunication  
Programs Division**  
Space & Electronics Group

One Space Park  
Redondo Beach, CA 90278  
310.812.4321

January 14, 2000

Dariusz Divsalar  
Jet Propulsion Laboratory  
California Institute of Technology  
M/S 238-420

Dear Dr. Divsalar,

I acknowledge that I am identified by C. Wayne Walker as Co-investigator to the investigation entitled "Power and Bandwidth Efficient Coded Modulation for Very High Data Rates," that is submitted by Dr. Dariusz Divsalar to the NASA Research Announcement 99-OSS-05 and that I intend to carry out all responsibilities identified for me in this proposal.

Sincerely,

A handwritten signature in black ink, appearing to read "C. Wayne Walker".

C. Wayne Walker, Ph.D.

TRW Inc.

## PROPOSAL TITLE:

Power and Bandwidth Efficient Coded Modulation for Very High Data Rates

## PROGRAM:

Advanced Cross-Enterprise Technology Development for NASA Missions

## Year 1 Budget Summary (\$K)

Includes optional Education/Public Outreach Proposal: ☒ YES ☐ NO

For Period from October 1, 2000, to September 30, 2001 (Year 1)

		NASA USE ONLY	
	A	B	C
1 <u>Direct Labor</u> (salaries, wages, and fringe benefits)	\$198.2		
2 <u>Other Direct Costs:</u>			
a. Subcontracts	\$88.0		
b. Services	\$0.0		
c. Equipment	\$0.0		
d. Supplies	\$0.0		
e. Travel	\$0.0		
f. Other (MPS & ADC)	\$99.2		
3 <u>Facilities and Administrative Costs</u>	\$22.3		
4 <u>Other Applicable Costs: (Award Fee)</u>	\$6.1		
5 <b>SUBTOTAL--Estimated Costs</b>	\$413.8		
6 <u>Less Proposed Cost Sharing (if any)</u>			
7 <u>Carryover Funds (if any)</u>			
a. Anticipated amount :			
b. Amount used to reduce budget			
8 <b>Total Estimated Costs</b>	\$413.8		XXXXXXXX
9 <b>APPROVED BUDGET</b>	XXXXXXXX	XXXXXXXX	

## PROPOSAL TITLE:

Power and Bandwidth Efficient Coded Modulation for Very High Data Rates

## PROGRAM:

Advanced Cross-Enterprise Technology Development for NASA Missions

## Year 2 Budget Summary (\$K)

Includes optional Education/Public Outreach Proposal: ☒ YES ☐ NO

For Period from October 1, 2001, to September 30, 2002 (Year 2)

	A	NASA USE ONLY	
		B	C
1 <u>Direct Labor</u> (salaries, wages, and fringe benefits)	\$156.8		
2 <u>Other Direct Costs:</u>			
a. Subcontracts	\$90.0		
b. Services	\$0.0		
c. Equipment	\$0.0		
d. Supplies	\$0.0		
e. Travel	\$0.0		
f. Other (MPS & ADC)	\$81.3		
3 <u>Facilities and Administrative Costs</u>	\$19.3		
4 <u>Other Applicable Costs: (Award Fee)</u>	\$4.9		
5 <b><u>SUBTOTAL--Estimated Costs</u></b>	<b>\$352.2</b>		
6 <u>Less Proposed Cost Sharing (if any)</u>			
7 <u>Carryover Funds (if any)</u>			
a. Anticipated amount :			
b. Amount used to reduce budget			
8 <b><u>Total Estimated Costs</u></b>	<b>\$352.2</b>		xxxxxxx
9 <b>APPROVED BUDGET</b>	xxxxxxx	xxxxxxx	

## PROPOSAL TITLE:

Power and Bandwidth Efficient Coded Modulation for Very High Data Rates

## PROGRAM:

Advanced Cross-Enterprise Technology Development for NASA Missions

## Year 3 Budget Summary (\$K)

Includes optional Education/Public Outreach Proposal: ☒ YES ☐ NO

For Period from October 1, 2002, to September 30, 2003 (Year 3)

		NASA USE ONLY	
	A	B	C
1 <u>Direct Labor</u> (salaries, wages, and fringe benefits)	\$138.3		
2 <u>Other Direct Costs:</u>			
a. Subcontracts	\$95.0		
b. Services	\$0.0		
c. Equipment	\$0.0		
d. Supplies	\$0.0		
e. Travel	\$0.0		
f. Other (MPS & ADC)	\$72.6		
3 <u>Facilities and Administrative Costs</u>	\$18.6		
4 <u>Other Applicable Costs: (Award Fee)</u>	\$4.2		
5 <b>SUBTOTAL--Estimated Costs</b>	\$328.7		
6 <u>Less Proposed Cost Sharing (if any)</u>			
7 <u>Carryover Funds (if any)</u>			
a. Anticipated amount :			
b. Amount used to reduce budget			
8 <b>Total Estimated Costs</b>	\$328.7		XXXXXX
9 <b>APPROVED BUDGET</b>	XXXXXX	XXXXXX	

## PROPOSAL TITLE:

Power and Bandwidth Efficient Coded Modulation for Very High Data Rates

## PROGRAM:

Advanced Cross-Enterprise Technology Development for NASA Missions

## Grand Total Budget Summary (\$K)

Includes optional Education/Public Outreach Proposal: ☒ YES ☐ NO

For Period from October 1, 2000, to September 30, 2003 (Years 1-3)

		NASA USE ONLY	
	A	B	C
1 <u>Direct Labor</u> (salaries, wages, and fringe benefits)	\$493.3		
2 <u>Other Direct Costs:</u>			
a. Subcontracts	\$273.0		
b. Services	\$0.0		
c. Equipment	\$0.0		
d. Supplies	\$0.0		
e. Travel	\$0.0		
f. Other (MPS & ADC)	\$253.0		
3 <u>Facilities and Administrative Costs</u>	\$60.2		
4 <u>Other Applicable Costs: (Award Fee)</u>	\$15.2		
5 <b><u>SUBTOTAL--Estimated Costs</u></b>	<b>\$1,094.7</b>		
6 <u>Less Proposed Cost Sharing (if any)</u>	\$0.0		
7 <u>Carryover Funds (if any)</u>			
a. Anticipated amount :			
b. Amount used to reduce budget			
8 <b><u>Total Estimated Costs</u></b>	<b>\$1,094.7</b>		XXXXXXX
9 <b>APPROVED BUDGET</b>	XXXXXXX	XXXXXXX	

### ***JPL Cost Accumulation System***

The NASA prime contract—NAS7-1407—is a Cost Reimbursable Award Fee type instrument. All costs incurred are billed to the Government on a 100% reimbursable basis. The costs to be charged for the proposed work must be consistent with contractual provisions and established procedures for costing under the current contract between NASA and Caltech. All charges developed at the Laboratory, including JPL applied burdens, are billed to the Government as direct charges at the rates in effect at the time the work is accomplished. Government audit is performed on a continuing basis by a Defense Contract Audit Agency team in residence.

Allocated Direct Costs (ADC) is the term for "JPL applied burdens." ADC includes activities (accounts) benefiting multiple tasks. The cost collection system groups common Allocated Direct Cost accounts into three groups. The groups are as follows:

- 1) Labor: Labor ADC
- 2) Procurement: Purchase Order ADC and Subcontract ADC.
- 3) General: a percentage of all subordinate costs on direct projects. (Similar to the General and Administrative expense in industry.)

Each grouping contains like functions or activities. The accounting process distributes these costs on a 100% reimbursable basis.

Multiple Program Support (MPS) is a distributed direct factor per JPL and accountable contractor workhour on respective program office direct accounts.

Labor—Employee Benefits consist of three labor fringe rates applied to direct labor as follows:

- Paid leave is a percentage of straight time labor costs.
- Vacation is a percentage of straight time labor cost and paid leave costs
- Benefits is a percentage of straight time and overtime labor costs, paid leave costs, and vacation costs.

Award Fee—the NASA/ Caltech contract for the operation of the federally funded research and development center (FFRDC) is a cost plus award fee contract. As such, all sponsors placing funds on contract contribute a small percentage of task order dollars toward the award fee.

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For this proposal the estimated costs have been built up in the same manner as above. However, their presentation in the required tables have been adapted in the following ways:

1. The costs for all three Employee Benefit components are included in the Direct Labor costs stated in this proposal.
2. Labor and Procurement ADC along with MPS costs are displayed in the "Other" category in the Other Direct Costs section.
3. Since the JPL General ADC costs are similar to G&A and are derived in the same fashion—a percentage of the subtotal of all costs—they are displayed in the Facilities and Administrative Costs section.
4. The Award Fee is displayed in the Other Applicable Costs section. The Award Fee annual percentage is 1.4% in Year 1, 1.4% in year 2, and 1.3% in subsequent fiscal years.